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THE ICS SEMINAR SERIES

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Automation Techniques for Post-silicon Debug of Timing Failures

The complexity of modern day electronic systems combined with nano-scale non-idealities have made “post-silicon” validation significantly cumbersome. At this stage few fabricated chips are verified for correct functionality in order to detect and fix the bugs which have escaped the design stage. The process has become time-consuming and expensive due to the costs of equipments and of (improved) silicon re-spins, the use of manual techniques, and the complicated nature of bugs in nano-scale technologies. Consequently, time-to-market and profit are directly at stake in many design domains.

One of the most challenging tasks in post-silicon validation is debugging for timing failures. Timing failures may be caused by factors such as (static) process variations and (transient) power droop. In this talk I will give an overview of our ongoing research towards automation of the debug process for timing failures. I will discuss our procedures for the following two cases (and mostly on the first case): 1) when the cause of timing failure is static process variations, and 2) when on-chip logic analyzers are used for capturing transient behavior and are intended to increase the "timing observability" inside the chip.

Biography:

Azadeh Davoodi has been an Assistant Professor of Electrical and Computer Engineering at the University of Wisconsin since 2006. She received her Ph.D. and M.S. at the University of Maryland and her B.Sc. from the University of Tehran in Electrical and Computer Engineering. Her research interest is in the area of Electronic Design Automation of Integrated Circuits for the nanometer technologies.

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