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Ultra–Low Power Logic Circuits: From Voltage–Mode to Current-Mode

In the last few years, subthreshold VLSI circuits have become very popular in ultra - low power applications such as distributed sensing, wearable computing, biomedical devices, green electronics. These applications typically constrain the power budget to a few tens of μWs and the supply voltage to a few hundreds of mV. Operation at such low power/voltage poses new interesting problems and challenges, and at the same time offers new opportunities to develop emerging applications, as well as to stimulate and enable new technologies and markets. In this talk, opportunities and challenges in the ultra-low power domain are presented in the context of current nanometer technologies, and are put in perspective. On the one hand, a comparison with standard superthreshold VLSI design is presented to highlight the most critical challenges that we will face in the next years. On the other hand, the impact of next technology generations is analyzed from the point of view of energy consumption and robustness.

Process/voltage/temperature variability and leakage are analyzed in a consistent framework to show how they ultimately affect ultra-low power/voltage operation, and practical limits to the voltage scaling and energy minimization will be identified by resorting to simple models. Other than exploring the energy/voltage boundary of subthreshold VLSI circuits, circuit design methodologies to push down the voltage lower bound are presented. Guidelines on how to systematically build ultra-low power standard cell libraries are also discussed. For the first time, robustness and yield are considered as further dimensions in the design space. In particular, the speech aims at clarifying the important role (usually neglected) that the voltage lower bound plays in real VLSI circuits, and its relation with the optimal voltage that minimizes the energy consumption.

As an alternative approach to ultra - low power computing, MOS Current Mode Logic (MCML) circuits are explored to understand limits and advantages over standard voltage-mode CMOS logic styles. Design issues arising in the ultra-low power realm with a power consumption in the order of pW-per-gate are discussed, and appropriate circuit techniques to allow reliable operation are ntroduced. Successful designs and state-of-the-art chips are presented to gain a clear understanding of the state-of-the-art, and which direction the research is moving to. Finally, open questions and aspects that require further investigation and new directions are highlighted.

Biography:

Massimo Alioto received the laurea degree in Electronics Engineering and the Ph.D. degree in Electrical Engineering from the University of Catania (Italy) in 1997 and 2001, respectively. In 2002, he joined the Dipartimento di Ingegneria dell'Informazione (DII) of the University of Siena as a Research Associate and in the same year as an Assistant Professor. In 2005 he was appointed Associate Professor of Electronics, and was engaged in the same faculty in 2006. In the summer of 2007, he was a Visiting Professor at EPFL-Lausanne (Switzerland). In 2009–2010, he is Visiting Professor at BWRC-UC Berkeley, investigating on ultra–low power circuits and wireless sensor nodes. Since 2001 he has been teaching undergraduate and graduate courses on advanced VLSI digital design, microelectronics and basic electronics.

He has authored or co-authored more than 140 publications on journals (50+, mostly IEEE Transactions) and conference proceedings. Two of them are among the 25 most downloaded TVLSI papers in 2007 (respectively 10th and 13th). He is coauthor of the book Model and Design of Bipolar and MOS Current ‐ Mode Logic: CML, ECL and SCL Digital Circuits (Springer, 2005). His primary research interests include the modeling and the optimized design of CMOS high ‐ performance, low ‐ power and ultra low ‐ power digital circuits, arithmetic and cryptographic circuits, interconnect modeling, design/modeling for variability tolerant and low–leakage VLSI circuits, circuit techniques for emerging technologies. He is the director of the Electronics Lab at University of Siena (site of Arezzo).

Prof. Alioto is an IEEE Senior Member and a member of the HiPEAC Network of Excellence. He is the Chair Elect of the "VLSI Systems and Applications" Technical Committee of the IEEE Circuits and Systems Society, for which he is also Distinguished Lecturer. He is regularly invited to give talks and tutorials to academic institutions, conferences and companies throughout the world. He has served as a member of various conference technical program committees (ISCAS, PATMOS, ICM, ICCD, CSIE) and Track Chair (ICECS, ISCAS, ICM, ICCD). He serves as Associate Editor of the IEEE Transactions on VLSI Systems, as well as of the Microelectronics Journal, the Integration-The VLSI journal and the Journal of Circuits, Systems, and Computers. He is Guest Editor of the Special Issue "Advances in oscillator analysis and design" of the Journal of Circuits, Systems, and Computers (2009), and Technical Program Chair for the ICM 2010 conference.

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