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THE ICS SEMINAR SERIES

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Application of Statistical Optimization for Process and Defect Tolerant Nanometer Scale Circuit Design

The technology scaling is helping to achieve higher integration density and frequency in each technology generation. However, at the same time there is an increasing unpredictability in the physical properties of semiconductor devices because of lack of manufacturing control. The future nanodevices are predicted to have even higher variability and defects due to manufacturing limitations. This necessitates a tighter integration of process and design flows. Due to statistical nature of the process variation, we must deal with statistical design methodology since developing such a methodology can reduce the impact of yield loss incurred due to high variability.

A major challenge is to develop efficient parametric yield optimization algorithms at different levels of abstraction in the design flow. In order to address this problem, my work has mainly focused on developing efficient tractable approximations that can be employed to overcome the high computational complexity of the statistical problem that are encountered during logic synthesis, post-synthesis optimization, circuit timing prediction and robust memory design.

In this talk, I will give a brief overview of my work in these areas. I will cover in details, the methods for yield constrained power optimization using joint design time and post-silicon tuning methods for logic and SRAM. I will also discuss the challenges associated with defect tolerance in future nanotechnologies and in particular a defect tolerant CMOS-CNT (Carbon Nano Tube) architecture using novel coding of Boolean functions.

Biography:

Ashish Kumar Singh received the B.Tech. degree in Computer Science from the Indian Institute of Technology, India, in 2001. He has received the M.S. degree from Royal Institute of Technology, Stockholm and Ph.D. degrees in electrical engineering from University of Texas, Austin, in 2003 and 2007 respectively. His research has been in the development of statistical and robust optimization algorithms for integrated circuit synthesis under manufacturing and operation uncertainty. He is currently in a postdoctoral research position with Professor Michael Orshansky at University of Texas, Austin. Prior to joining the postdoctoral position he held the position of senior member of technical staff at Magma Design Automation. He has received the Best Paper Award at 2006 International Conference for Computer Aided Design.

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